Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts offered are recommended only as guidelines.

OUT and nOUT are low impedance following outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 43 and 44 present two different designs. They are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designer simulate to guarantee compatibility across all printed circuit and clock component process variations.

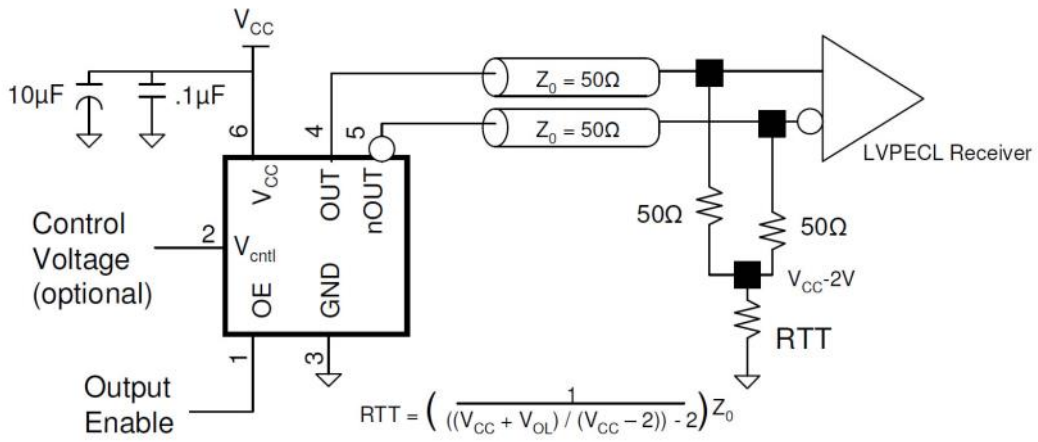


Figure 43 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

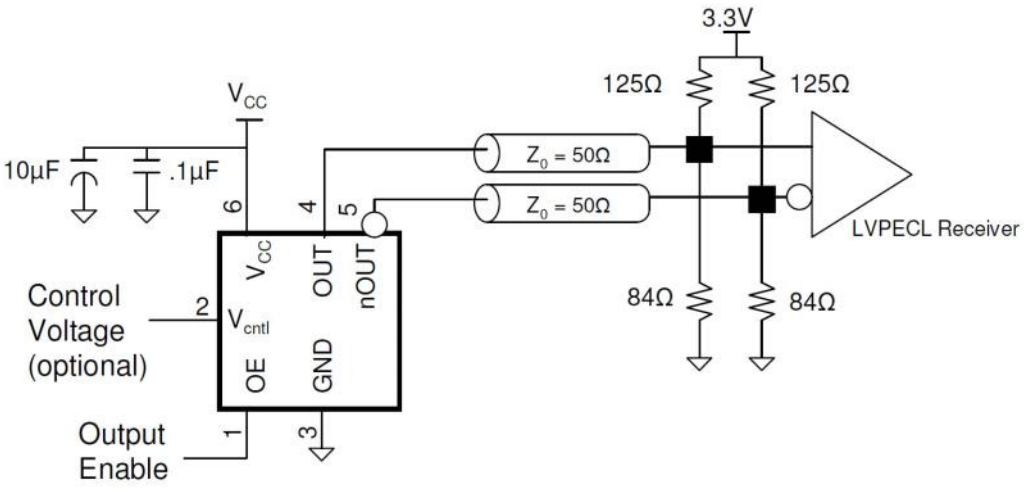


Figure 44 Alternate 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

Termination for 2.5V LVPECL Output

Figures 45-47 show examples of termination for 2.5V LVPECL drivers. These terminations are equivalent to terminating 50Ω to VCC-2V. For VCC = 2.5V, the VCC-2V is very close to ground level. The 18Ω in figure 46 can be eliminated and termination is shown in figure 47.

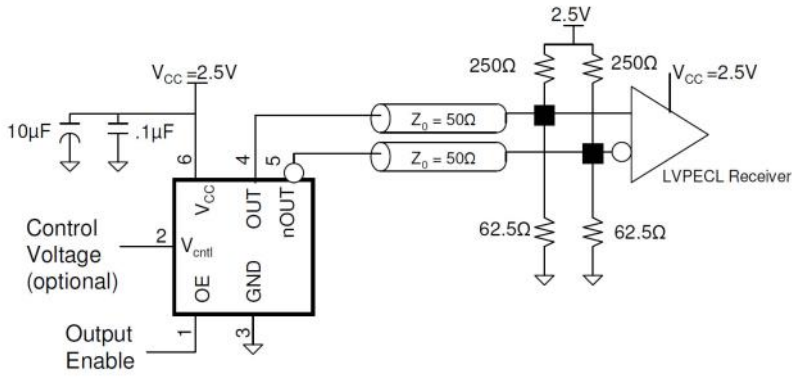


Figure 45 2.5V LVPECL XO Driver Termination Example

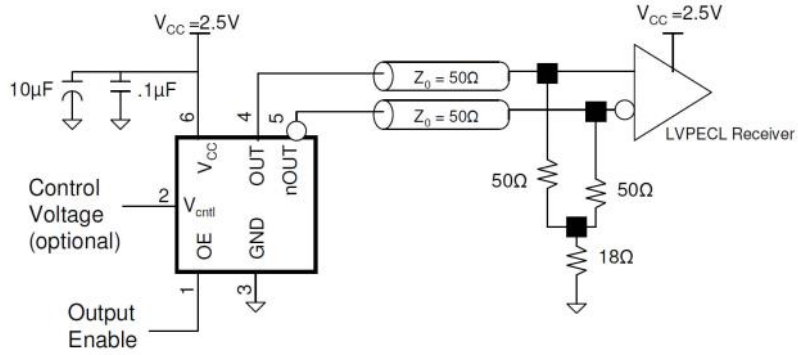


Figure 46 Alternate 2.5V LVPECL XO Driver Termination Example

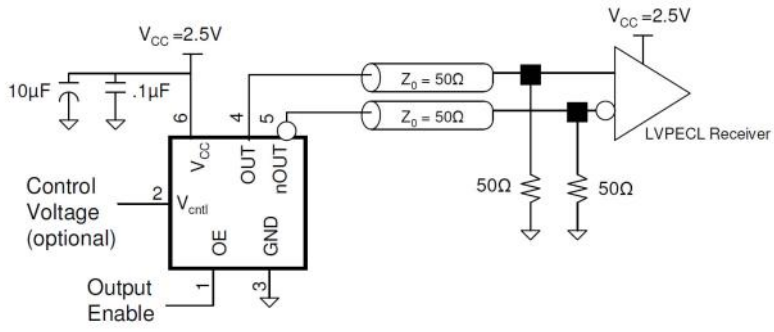


Figure 47 Alternate 2.5V LVPECL XO Driver Termination Example

Termination for 3.3V and 2.5V LVDS Output

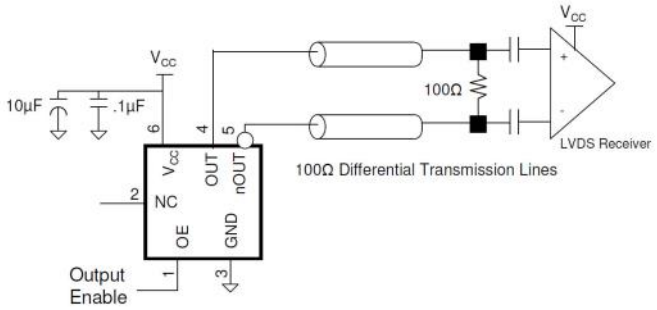
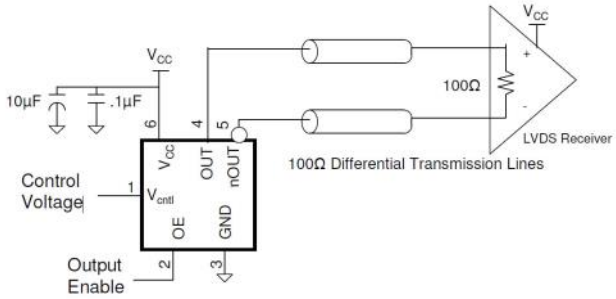


Figure 48 Termination for 3.3V and 2.5V LVDS Output



Note: A general LVDS interface is presented in Figure 49. In a 100Ω differential transmission line environment, the LVDS drivers require a matched load termination of 100Ω near the receiver input. For a multiple LVDS output buffer, if all outputs are not used, it is recommended that the unused outputs be terminated.

Figure 49 3.3V and 2.5V LVDS XO Application Schematic & Power Supply Decoupling

Termination for HCSL Output

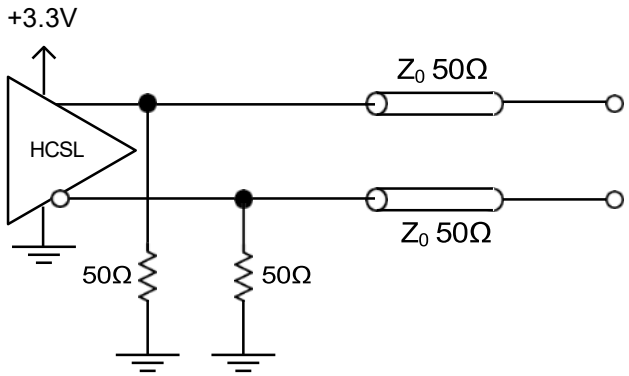
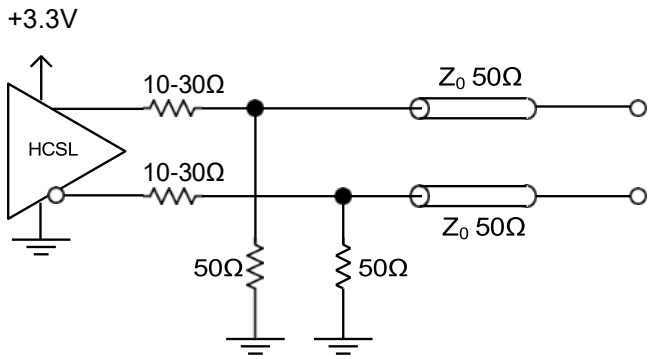


Figure 50 Termination for HCSL Output



Note: In some cases a 10-30Ω series resistor is used to help reduce overshoot.

Figure 51 Alternate termination for HCSL Output