

**FR4 PCB BASED 6PAD SMD CMOS/LVDS/LVPECL VCXO (14.3 x 8.7 x 5.5mm)**
**FEATURES:**

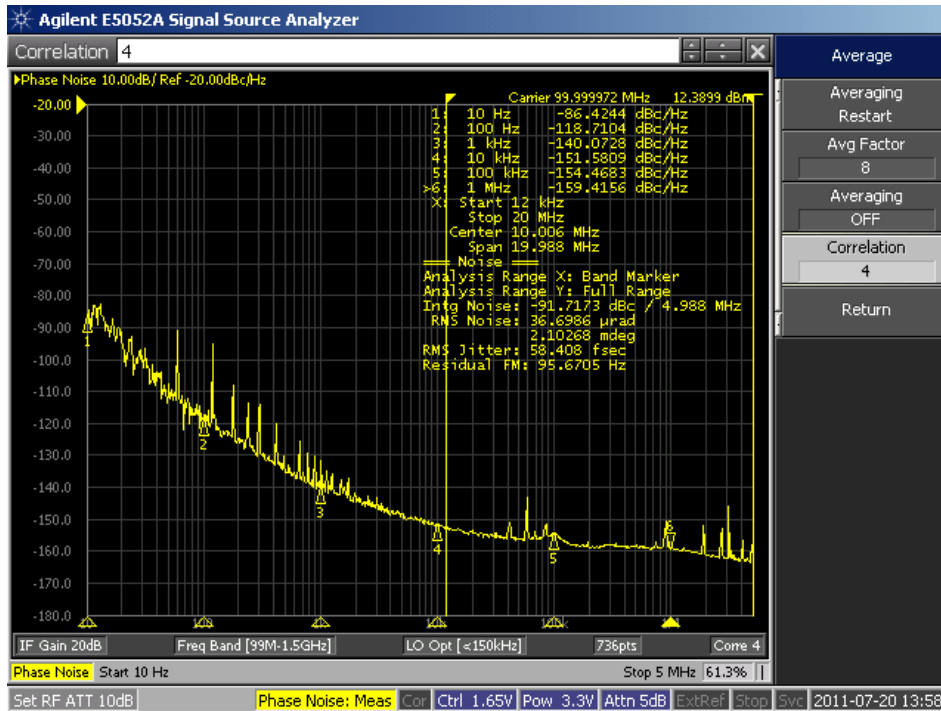
- CMOS/LVDS/LVPECL HIGH FREQUENCY RANGE
- LOW JITTER / LOW CURRENT
- SUITABLE FOR REFLOW


**■ SPECIFICATION**

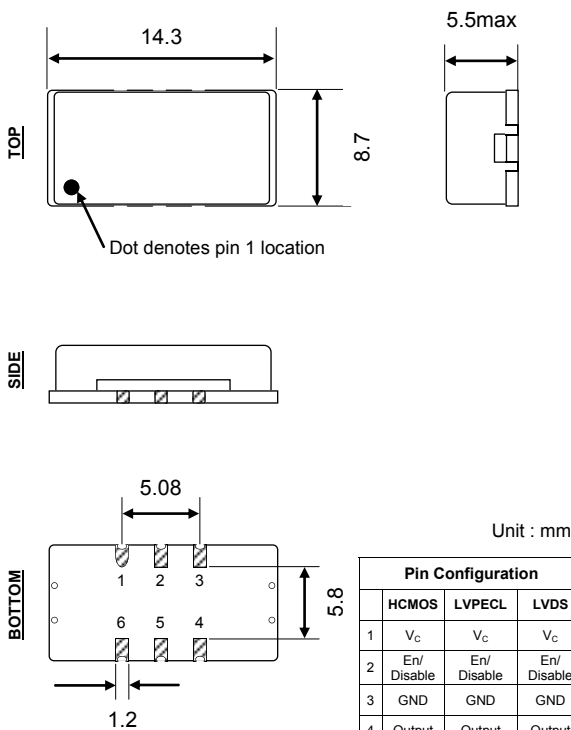
PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE	
FREQUENCY RANGE		0.001		800.000	MHz		
FREQUENCY STABILITY		±10		±100	ppm	See P/N guide for other options	
OPERATING TEMPERATURE RANGE		-40		85	°C	See P/N guide for other options	
STORAGE TEMPERATURE RANGE		-55		105	°C		
SUPPLY VOLTAGE ±10%		3.3		5.0	V	See P/N guide for other options	
SUPPLY CURRENT	CMOS	10		100	mA		
	LVDS	15		65	mA		
	LVPECL	15		80	mA		
OUTPUT	LOAD	CMOS		15	pF		
		LVDS		100	Ω	Output - Complementary Output	
		LVPECL		50	Ω	To V <sub>DD</sub> - 2V	
	LEVEL	CMOS (V <sub>OH</sub> )	0.9 x V <sub>DD</sub>			V	
		CMOS (V <sub>OL</sub> )			0.1 x V <sub>DD</sub>	V	
		LVDS (V <sub>OH</sub> )		1.4	1.6	V	
		LVDS (V <sub>OL</sub> )	0.9	1.1		V	
		LVPECL (V <sub>OH</sub> )		V <sub>DD</sub> - 1.025		V	
		LVPECL (V <sub>OL</sub> )		V <sub>DD</sub> - 1.62		V	
	SYMMETRY (DUTY CYCLE)	CMOS	40		60	%	
		LVDS	40		60	%	
		LVPECL	45		55	%	
	RISE AND FALL TIME (Tr/Tf)	CMOS			10	nS	
		LVDS		0.3	1.0	nS	
		LVPECL		0.3	1.0	nS	
START-UP TIME					mS		
FREQUENCY DEVIATION		±50		±200	ppm	See P/N guide for other options	
CONTROL VOLTAGE	3.3V	0.15		3.15	V		
	5.0V	0		5	V		
LINEARITY				10	%		
INPUT IMPEDANCE		100			kΩ		
AGING @ 25°C + 3°C				±3.0	ppm	@ 1 <sup>st</sup> year	
PHASE JITTER RMS	FUNDAMENTAL		0.5	1.0	pS	@ 12kHz ~ 20MHz offset	
	PLL (3.3V)			4.0	pS		
PHASE NOISE			-154.4683		dBc	@ 100MHz	

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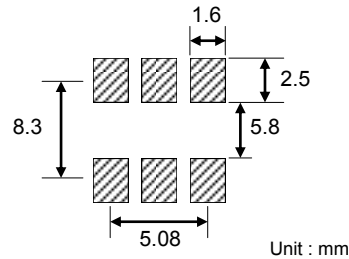
## ■ PHASE NOISE (TYPICAL) @ 100MHz (0°C to 70°C)



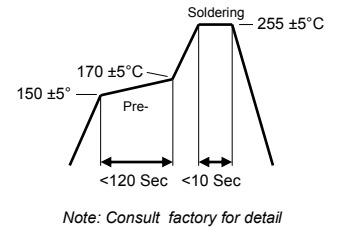
## ■ PACKAGE DIMENSIONS



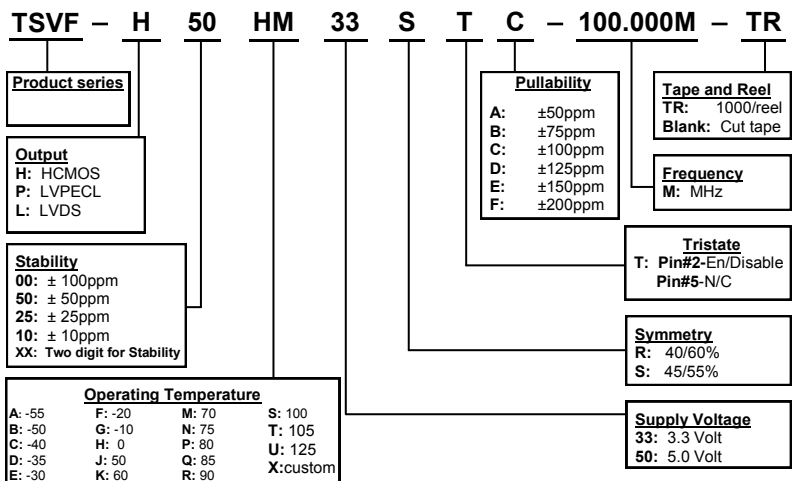
## ■ SOLDER PATTERN



## ■ REFLOW PROFILE



## ■ PART NUMBERING GUIDE



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