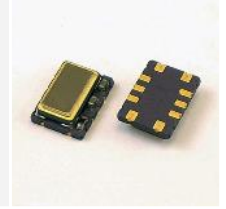


CERAMIC SMD TCXO / VCTCXO (7.0 x 5.0 x 2.0mm)
FEATURES

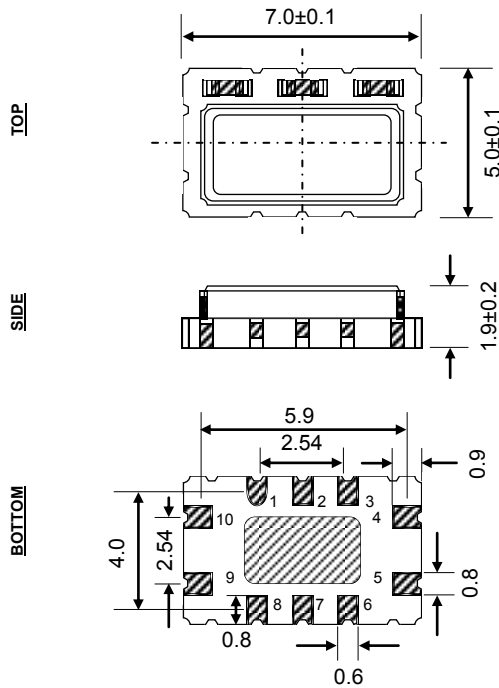
- HIGH STABILITY UP TO $\pm 0.05\text{ppm}$
- LOW PHASE NOISE
- USED FOR **FEMTOCELL** APPLICATION


■ SPECIFICATION

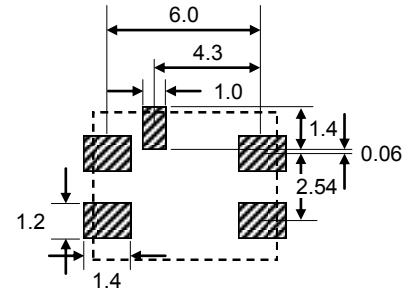
PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE	
FREQUENCY RANGE		5		40	MHz		
STANDARD FREQUENCIES	CMOS	5M, 6.4M, 8.192M, 10M, 12.5M, 12.8M, 16M, 16.384M, 19.44M, 25M					
	CSW	8.192M, 10M, 12.5M, 12.8M, 16M, 16.384M, 19.44M, 25M					
FREQUENCY TOLERANCE				± 2.0	ppm		
FREQUENCY STABILITY	vs. TEMPERATURE RANGE	± 0.05		± 0.5	ppm	See P/N guide for other options	
	vs. LOAD $\pm 10\%$			± 0.2	ppm		
	vs. SUPPLY VOLTAGE $\pm 5\%$			± 0.5	ppm		
	vs. AGING			± 1.0	ppm		
OPERATING TEMPERATURE RANGE		-40		+85	$^{\circ}\text{C}$	See P/N guide for other options	
STORAGE TEMPERATURE RANGE		-55		-125	$^{\circ}\text{C}$		
SUPPLY VOLTAGE $\pm 5\%$		3.3		5.0	V		
SUPPLY CURRENT	CMOS			6	mA		
	CSW			3.5	mA		
OUTPUT	LOAD	CMOS	15pF				
		CSW	10k Ω //10pF				
	LEVEL	CMOS (V_{OH})	$V_{DD} \times 0.90$			V	
		CMOS (V_{OL})			$V_{DD} \times 0.10$	V	
		CSW	0.8			V_{P-P}	
	SYMMETRY (DUTY CYCLE)		45		55	%	For CMOS
	RISE AND FALL TIME (T_r/T_f)				10	nS	For CMOS
	START-UP TIME				2.0	mS	
STAND-BY VOLTAGE	ENABLE (V_{IH})	$0.7 \times V_{DD}$			V		
	DISABLE (V_{IL})			$0.3 \times V_{DD}$	V		
FREQUENCY DEVIATION		± 5.0		± 12.0	ppm	See P/N guide for other options	
CONTROL VOLTAGE		0.5		2.5	V		
V_c INPUT IMPEDANCE		100			k Ω		
PHASE NOISE	100Hz			-120	dBc/Hz	@ 12.8MHz	
	1kHz			-140	dBc/Hz		
	10kHz			-148	dBc/Hz		

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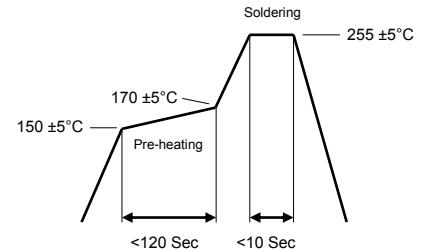
PACKAGE DIMENSIONS



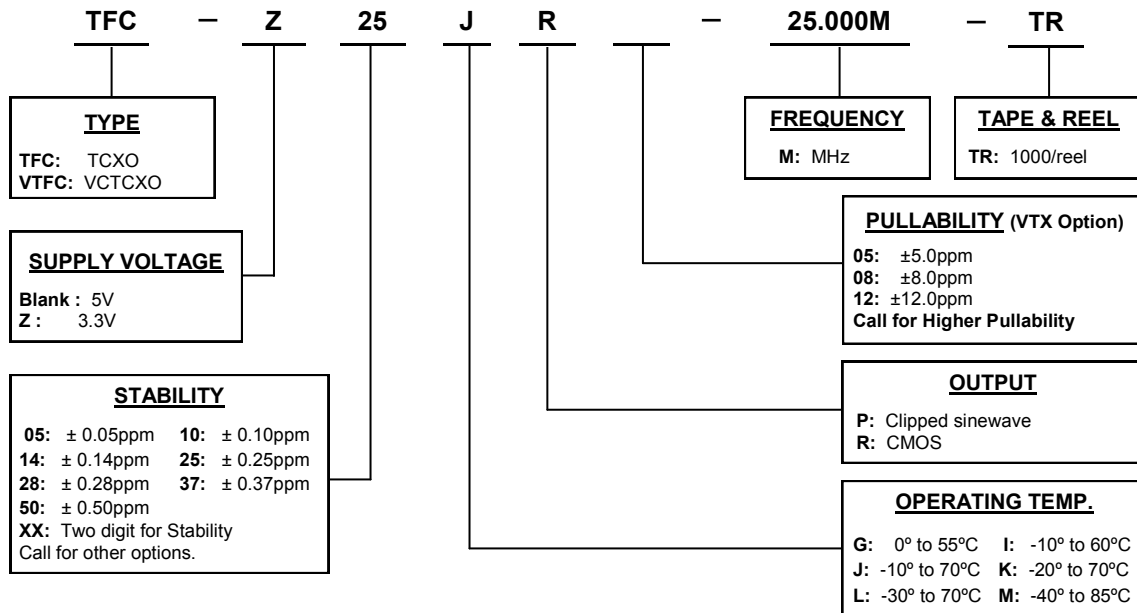
SOLDER PATTERN



REFLOW PROFILE



PART NUMBERING GUIDE



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