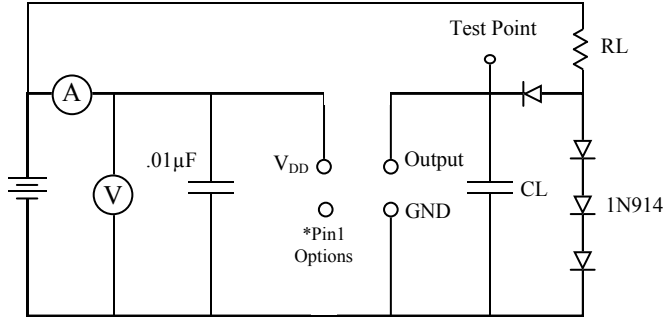
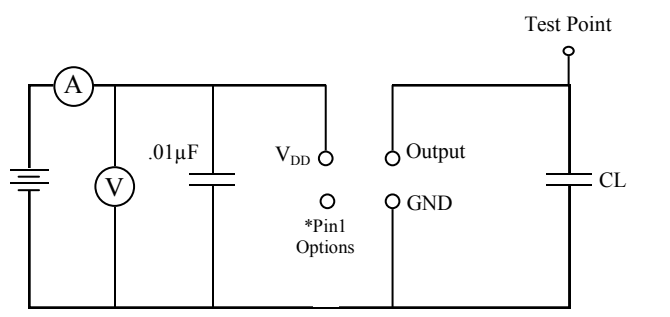
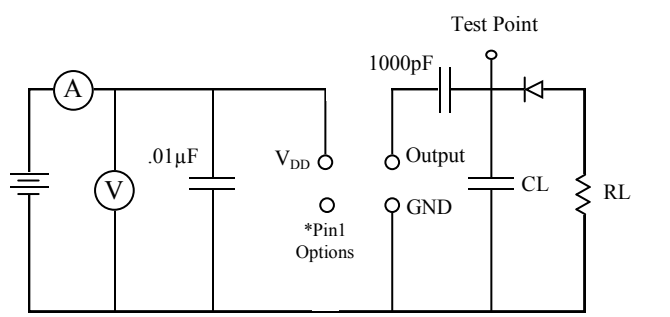
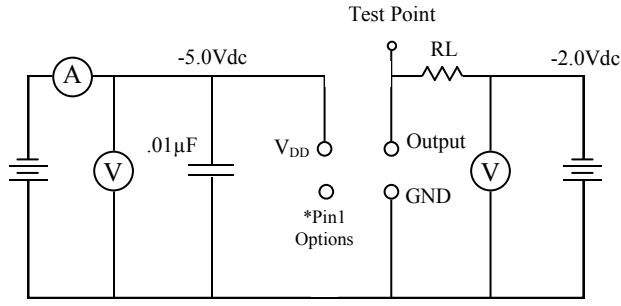
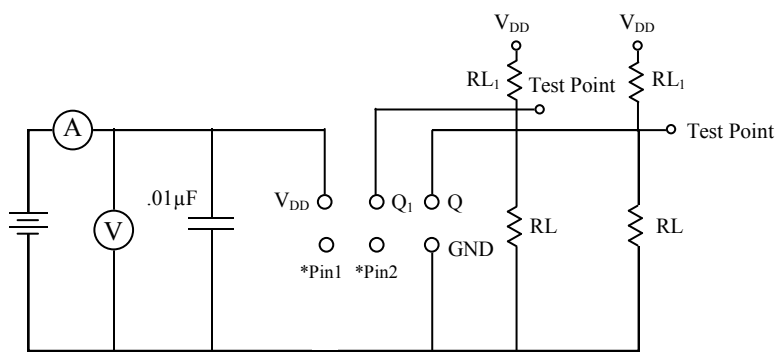
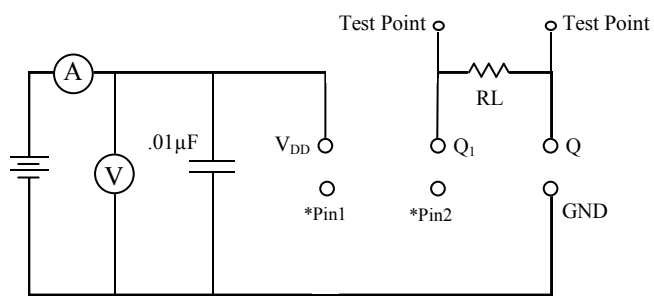


<h2>TTL</h2>	 <p>The diagram shows a TTL test circuit. On the left, a battery is connected in series with an ammeter (A) and a voltmeter (V). A .01μF capacitor is connected in parallel with the voltmeter. The circuit is powered by V<sub>DD</sub>. The output of the device is connected to a test point, which is also connected to a load resistor (RL). A diode and a capacitor (CL) are connected in parallel between the test point and ground. The diode is oriented with its cathode towards the test point. The capacitor CL is connected between the test point and ground. The load resistor RL is connected between the test point and ground. The output is also connected to a diode and a capacitor (CL) in parallel, with the diode oriented with its cathode towards the output and the capacitor CL connected to ground. The load resistor RL is connected between the test point and ground. The output is also connected to a diode and a capacitor (CL) in parallel, with the diode oriented with its cathode towards the output and the capacitor CL connected to ground. The load resistor RL is connected between the test point and ground.</p> <p> <math>RL = 2.0k\Omega</math> (2TTL) / <math>RL = 820\Omega</math> (2TTL)  <math>RL = 390\Omega</math> (2TTL) / <math>CL = 15pF</math> </p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin-left: auto; margin-right: auto;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div>
<h2>HCMOS</h2>	 <p>The diagram shows an HCMOS test circuit. On the left, a battery is connected in series with an ammeter (A) and a voltmeter (V). A .01μF capacitor is connected in parallel with the voltmeter. The circuit is powered by V<sub>DD</sub>. The output of the device is connected to a test point, which is also connected to a load capacitor (CL). The output is also connected to ground. The load capacitor CL is connected between the test point and ground.</p> <p><math>CL = 15pF</math></p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin-left: auto; margin-right: auto;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div>
<h2>Sine Wave</h2>	 <p>The diagram shows a Sine Wave test circuit. On the left, a battery is connected in series with an ammeter (A) and a voltmeter (V). A .01μF capacitor is connected in parallel with the voltmeter. The circuit is powered by V<sub>DD</sub>. The output of the device is connected to a test point, which is also connected to a load resistor (RL). A diode and a capacitor (CL) are connected in parallel between the test point and ground. The diode is oriented with its cathode towards the test point. The capacitor CL is connected between the test point and ground. The load resistor RL is connected between the test point and ground. The output is also connected to a diode and a capacitor (CL) in parallel, with the diode oriented with its cathode towards the output and the capacitor CL connected to ground. The load resistor RL is connected between the test point and ground.</p> <p> <math>RL = 10k\Omega</math> / <math>CL = 10pF</math> </p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin-left: auto; margin-right: auto;"> <p>*Pin 1 Options: a. NC b. Tri-State c. VC</p> </div>

<b>ECL</b>	 <p>The diagram shows a test circuit for ECL. On the left, a current source (A) and a voltage source (V) are connected to a <math>-5.0V_{dc}</math> supply. A <math>.01\mu F</math> capacitor is connected to the <math>V_{DD}</math> pin. The output is connected to a load resistor (RL) and a <math>-2.0V_{dc}</math> supply. A voltage source (V) is connected across the load resistor. A "Test Point" is indicated at the output. The <math>V_{DD}</math> pin is labeled with "*Pin1 Options".</p> <p><math>RL = 50\Omega</math></p> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: auto;"> <p>*Pin 1 Options:</p> <ul style="list-style-type: none"> <li>a. Complementary Output</li> <li>b. NC</li> <li>c. Tri-State</li> <li>d. VC</li> </ul> </div>												
<b>LVPECL</b>	 <p>The diagram shows a test circuit for LVPECL. It features a current source (A) and a voltage source (V) connected to a <math>V_{DD}</math> supply. A <math>.01\mu F</math> capacitor is connected to the <math>V_{DD}</math> pin. The output is connected to a load resistor (RL) and a <math>V_{DD}</math> supply. A voltage source (V) is connected across the load resistor. A "Test Point" is indicated at the output. The <math>V_{DD}</math> pin is labeled with "*Pin1 Options".</p> <p><math>RL = 82\Omega</math> <math>RL1 = 124\Omega</math> <math>Q = Output</math> <math>Q_1 = Complementary Output</math></p> <table border="1" style="margin: auto; border-collapse: collapse;"> <thead> <tr> <th colspan="3">*Pin Option</th> </tr> </thead> <tbody> <tr> <td></td> <td>OSC</td> <td>VCXO</td> </tr> <tr> <td>Pin 1</td> <td>Tri-State</td> <td><math>V_C</math></td> </tr> <tr> <td>Pin 2</td> <td>NC</td> <td>Tri-State</td> </tr> </tbody> </table>	*Pin Option				OSC	VCXO	Pin 1	Tri-State	$V_C$	Pin 2	NC	Tri-State
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	OSC	VCXO											
Pin 1	Tri-State	$V_C$											
Pin 2	NC	Tri-State											
<b>LVDS</b>	 <p>The diagram shows a test circuit for LVDS. It features a current source (A) and a voltage source (V) connected to a <math>V_{DD}</math> supply. A <math>.01\mu F</math> capacitor is connected to the <math>V_{DD}</math> pin. The output is connected to a load resistor (RL) and a <math>V_{DD}</math> supply. A voltage source (V) is connected across the load resistor. A "Test Point" is indicated at the output. The <math>V_{DD}</math> pin is labeled with "*Pin1 Options".</p> <p><math>RL = 100\Omega</math> <math>Q = Output</math> <math>Q_1 = Complementary Output</math></p> <table border="1" style="margin: auto; border-collapse: collapse;"> <thead> <tr> <th colspan="3">*Pin Option</th> </tr> </thead> <tbody> <tr> <td></td> <td>OSC</td> <td>VCXO</td> </tr> <tr> <td>Pin 1</td> <td>Tri-State</td> <td><math>V_C</math></td> </tr> <tr> <td>Pin 2</td> <td>NC</td> <td>Tri-State</td> </tr> </tbody> </table>	*Pin Option				OSC	VCXO	Pin 1	Tri-State	$V_C$	Pin 2	NC	Tri-State
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