

1.8V HCMOS SMD VCXO

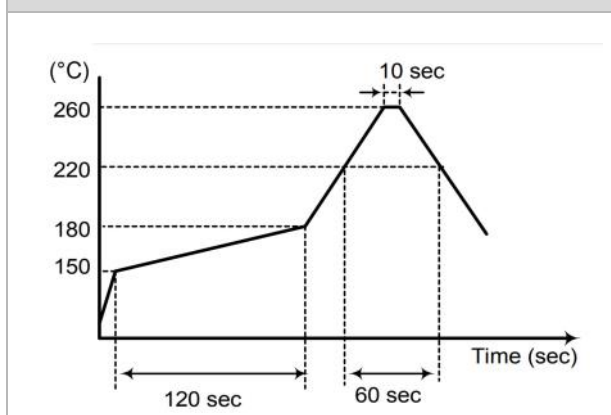
FEATURES:

- 1.8 VOLT LVCMOS OUTPUT
- LOW JITTER

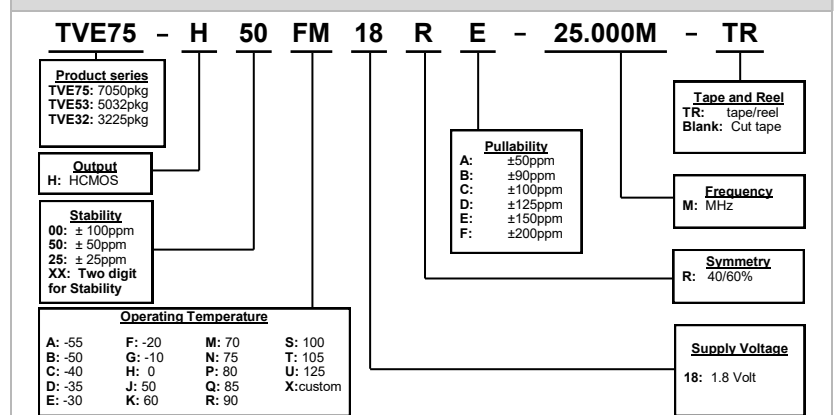
■ SPECIFICATION

PARAMETER		TVE75	TVE53	TVE32	NOTE
FREQUENCY RANGE		20MHz to 40MHz			See P/N guide for options
FREQUENCY STABILITY vs OPER. TEMP.		±25ppm, ±50ppm, ±100ppm			See P/N guide for options
OPERATING TEMPERATURE RANGE		0°C to 70°C / -20°C to 70°C / -40°C to 85°C			See P/N guide for options
STORAGE TEMPERATURE RANGE		-40°C to 90°C			
SUPPLY VOLTAGE (±5%)		1.80V (1.71V to 1.89V)			
SUPPLY CURRENT		20 max	15 max	10 max	
OUTPUT	LOGIC FAMILY	LVCMOS			
	LOAD	15pF			
	LEVEL LOGIC '1' (V _{OH})	0.9 x V _{DD} min			
	LEVEL LOGIC '0' (V _{OL})	0.1 x V _{DD} max			
	SYMMETRY (DUTY CYCLE)	40/60%			
	RISE AND FALL TIME (Tr/Tf)	10nS max			@ Load = 15pF
FREQUENCY DEVIATION		±150 min	±100 min	±90 min	See P/N guide for options
CONTROL VOLTAGE		0 to 1.8V (0.9V center)			
SLOPE		Positive			
LINEARITY		20% max			
MODULATION BANDWIDTH @-3dB		100KHz typ.			
INPUT IMPEDANCE		10MΩ min			
AGING @ 25°C		±3ppm max			for 1 st year
PHASE JITTER RMS		1.0pS max			@ 12kHz ~ 20MHz offset
ENABLE VOLTAGE (VIH)		0.8 x VDD ≤ VIH ≤ VDD or N/C			
DISABLE VOLTAGE (VIL)		VIL ≤ 0.2 x VDD			

■ REFLOW PROFILE



■ PART NUMBERING GUIDE



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■ PACKAGE DIMENSIONS (mm)

TVE75

Pin Configuration	
1	V _{Con}
2	En/Dis
3	GND
4	OUTPUT
5	N/C
6	V _{DD}

SOLDER PATTERN

A capacitor of value 0.1μF or 0.01μF between V_{DD} and GND is recommended.

TVE53

Pin Configuration	
1	V _{Con}
2	En/Dis
3	GND
4	OUTPUT
5	N/C
6	V _{DD}

SOLDER PATTERN

A capacitor of value 0.1μF or 0.01μF between V_{DD} and GND is recommended.

TVE32

Pin Configuration	
1	V _{Con}
2	En/Dis
3	GND
4	OUTPUT
5	N/C
6	V _{DD}

SOLDER PATTERN

A capacitor of value 0.1μF or 0.01μF between V_{DD} and GND is recommended.